

REMARKS

Status of Claims:

Claims 1-3 have been canceled and new claims 4-10 have been added. Thus, claims 4-10 are present for examination.

Rejection under Sec. 112:

The rejection of claims 1-3 under Sec. 112 as stated Par. 4 of the office action is rendered moot by cancellation of the rejected claims. The newly added claims are free from any such Sec. 112 rejection.

Prior Art Rejection:

Claims 1-3 stand rejected under 35 U.S.C. § 102 as anticipated by Tsutsui. This rejection is likewise rendered moot by cancellation of the rejected claims.

The newly submitted claims closely parallel the device claims contained within the issued '240 patent. As a representative example, applicant's newly submitted claim 4 recites:

4. (New) A semiconductor device manufacturing method comprising the steps of:

manufacturing wafers in a manufacturing line using predetermined manufacturing processes, each of said wafers having a plurality of semiconductor chips provided therein in a grid-like arrangement;

testing said plurality of semiconductor chips for electric characteristics thereof;

writing into each of said plurality of semiconductor chips, information of a chip position on said wafer associated with said testing;

storing a first test result from said testing step and storing said chip position information that is associated with said first test result;

dividing said wafer into respective ones of said semiconductor chips to produce semiconductor devices each sealed in a package;

testing each of said semiconductor devices for its electric characteristics to produce second test results;

detecting stored position information of each of said semiconductor devices associated with said second test results after said semiconductor device has been sealed in a package;

storing said second test results and said associated information of said semiconductor device position; and

mapping the distribution of failures corresponding to a wafer by combining position information of those chips determined to be faulty in said semiconductor chip testing step and position information of those semiconductor devices determined to be faulty in said semiconductor devices testing step, based on said first test result, said second test result and said information of chip position and semiconductor device position;

determining a cause of failures based on said distribution of failures.

It is submitted that applicant's claim 4 distinguishes over the Tsutsui reference at least because of the underlined portions of claim 4 indicted above. Tsutsui uses a physical inspection test (in addition to an electrical test) and does not test the chips before and after division into semiconductor devices. The remaining independent claims are also deemed patentable based on analogous reasoning. Applicant's dependent claims are deemed patentable at least by virtue of their dependency.

In order for a reference to be utilized as an anticipatory reference under the provisions of 35 U.S.C. § 102, the reference must disclose each and every claim limitation. This is certainly not the case here, and thus the Sec. 102 rejection must be withdrawn.

Conclusion:

It is submitted that the application is now in condition for allowance and an early indication of same is earnestly solicited.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 19-0741.

Respectfully submitted,

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